CLAIMS:

1. A method for power-gating a column read amplifier comprising N-channel pass transistors in a memory array, said method comprising:

applying a column read signal to said read amplifier of substantially a supply voltage level in a Select Mode of operation;

applying a column read signal to said read amplifier of substantially a reference voltage level in a Deselect Mode of operation; and

applying a column read signal to said read amplifier of less than said reference voltage level in a Sleep Mode of operation.

2. A method for power-gating a column read amplifier comprising P-channel pass transistors in a memory array, said method comprising:

applying a column read signal to said read amplifier of substantially a reference voltage level in a Select Mode of operation;

applying a column read signal to said read amplifier of substantially a supply voltage level in a Deselect Mode of operation; and

applying a column read signal to said read amplifier of more than said supply voltage level in a Sleep Mode of operation.

3. A power-gated column read amplifier having Select, Deselect and Sleep states thereof comprising:

first and second transistors having a first terminal thereof coupled to a reference voltage level and a control terminal thereof coupled to one of a pair of complementary bit lines;

third and fourth transistors in series with said first and second transistors respectively for selectively coupling one of a pair of complementary read data lines to second terminals of said first and second transistors in response to a column read signal coupled to a control terminal of said third and fourth transistors

whereby in a Sleep Mode of operation, said column read signal is at a level below that of said reference voltage level.

4. The power-gated column read amplifier of claim 3 wherein, in a Select Mode of operation, said column read signal is substantially at a supply voltage level.

5. The power-gated column read amplifier of claim 3 wherein, in a Deselect Mode of operation, said column read signal is substantially at said reference voltage level.

6. The power-gated column read amplifier of claim 3 wherein said first, second, third and fourth transistors comprise MOS transistors.

7. The power-gated column read amplifier of claim 6 wherein said third and fourth transistors comprise N-channel transistors.

8. A power-gated column read amplifier having Select, Deselect and Sleep states thereof comprising:

first and second transistors having a first terminal thereof coupled to a supply voltage level and a control terminal thereof coupled to one of a pair of complementary bit lines;

third and fourth transistors in series with said first and second transistors respectively for selectively coupling one of a pair of complementary read data lines to second terminals of said first and second transistors in response to a column read signal coupled to a control terminal of said third and fourth transistors

whereby in a Sleep Mode of operation, said column read signal is at a level above that of said supply voltage level.

9. The power-gated column read amplifier of claim 8 wherein, in a Select Mode of operation, said column read signal is substantially at a reference voltage level.

10. The power-gated column read amplifier of claim 8 wherein, in a Deselect Mode of operation, said column read signal is substantially at said supply voltage level.

11. The power-gated column read amplifier of claim 8 wherein said first, second, third and fourth transistors comprise MOS transistors.

12. The power-gated column read amplifier of claim 8 wherein said third and fourth transistors comprise P-channel transistors.

13. An integrated circuit device including a memory array comprising a power-gated column read amplifier having Select, Deselect and Sleep operational modes thereof, said device comprising:

a column read signal input to said power-gated column read amplifier for receiving a column read signal comprising three distinct voltage level states,

each of said voltage level states corresponding to one of said Select, Deselect and Sleep operational modes.

14. The integrated circuit device of claim 13 wherein said power-gated column read amplifier comprises:

first and second transistors having a first terminal thereof coupled to a reference voltage level and a control terminal thereof coupled to one of a pair of complementary bit lines; and

third and fourth transistors in series with said first and second transistors respectively for selectively coupling one of a pair of complementary read data lines to second terminals of said first and second transistors in response to said column read signal coupled to a control terminal of said third and fourth transistors.

15. The integrated circuit device of claim 14 wherein, in said Sleep operational mode, said column read signal is at a level below that of said reference voltage level.

16. The integrated circuit device of claim 14 wherein, in said Select operational mode, said column read signal is substantially at a supply voltage level.

17. The integrated circuit device of claim 14 wherein, in said Deselect operational mode, said column read signal is substantially at said reference voltage level.

18. The integrated circuit device of claim 14 wherein said first, second, third and fourth transistors comprise MOS transistors.

19. The integrated circuit device of claim 18 wherein said third and fourth transistors comprise N-channel transistors.

20. The integrated circuit device of claim 13 wherein said power-gated column read amplifier comprises:

first and second transistors having a first terminal thereof coupled to a supply voltage level and a control terminal thereof coupled to one of a pair of complementary bit lines; and

third and fourth transistors in series with said first and second transistors respectively for selectively coupling one of a pair of complementary read data lines to second terminals of said first and second transistors in response to said column read signal coupled to a control terminal of said third and fourth transistors

21. The integrated circuit device of claim 20 wherein, in said Sleep operational mode, said column read signal is at a level above that of said supply voltage level.

22. The integrated circuit device of claim 20 wherein, in said Select operational mode, said column read signal is at a level substantially that of a reference voltage level.

23. The integrated circuit device of claim 20 wherein, in said Deselect operational mode, said column read signal is substantially at said supply voltage level.

24. The integrated circuit device of claim 20 wherein said first, second, third and fourth transistors comprise MOS transistors.

25. The integrated circuit device of claim 20 wherein said third and fourth transistors comprise P-channel transistors.